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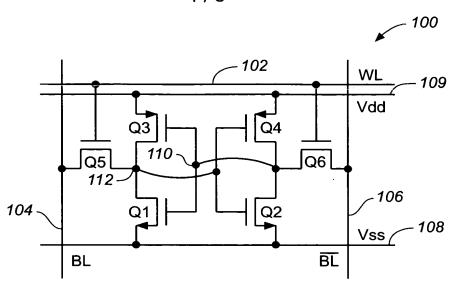


FIG._1 (PRIOR ART)

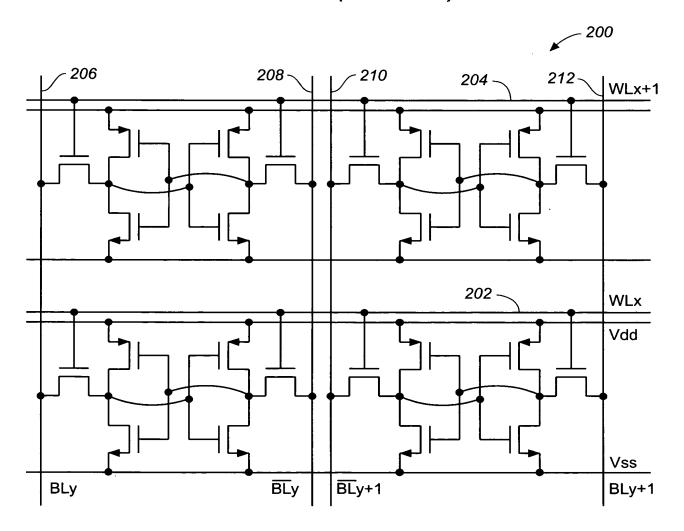
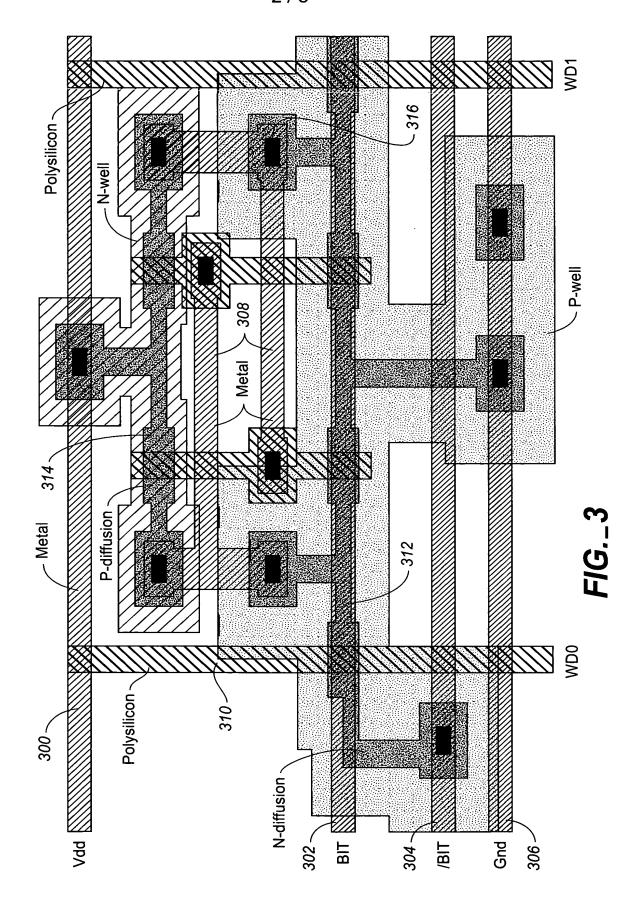


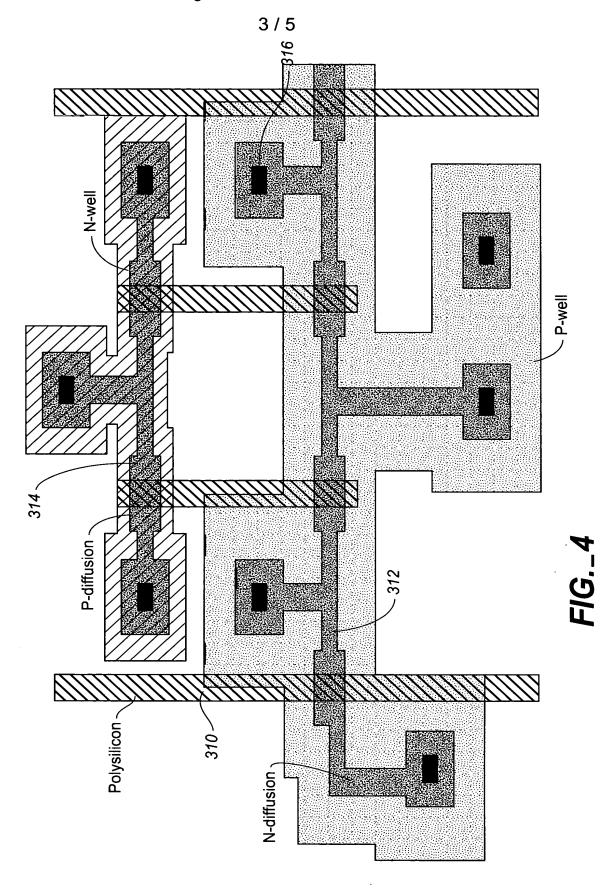
FIG._2 (PRIOR ART)

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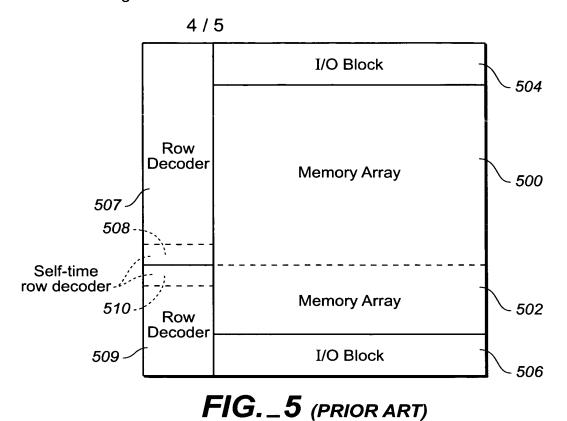
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Dummy Dummy bit cell(s) sense amp 612 614 Self-time row decoder I/O Block 610 -604 Self-time row decoder activation signal path 620-Dummy bitcell bitline path to the dummy sense amp 626 **Memory Array** 600 Row 607 Decoder 609 Row Dummy bitcell bitline path Decoder to the dummy sense amp 624 Self-time row decoder activation signal path 622 **Memory Array** 602 608 I/O Block Self-time 606 row decoder - 616 618 **Dummy Dummy** sense amp bit cell(s)

FIG._6

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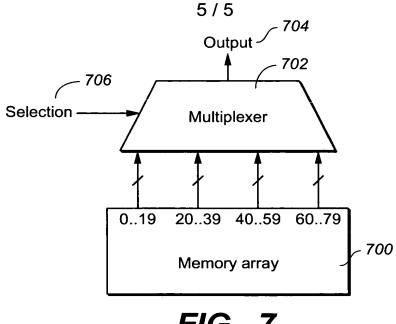
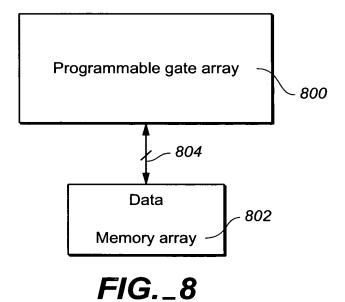


FIG._7



- 902 - 906 - 900 - 908 - 904 Layout Description Fabrication **Editor** Compiler process

FIG._9